ALMA Weekly Progress Report
22nd August 2003

Name: Jeff Mangum
AEG Group

ATF:

1. Continued characterization of VertexRSI antenna positioning system.
2. Continued analysis of VertexRSI tiltmeter system. Preparing report on results for VertexRSI.
3. Continued with optical pointing measurements of VertexRSI antenna.
4. Reviewed AEC and NAOJ prototype antenna schedules with Stanghellini and Ukita, respectively.

Name: John Effland
IPT: Front End

We held conference call with the Electronics Group in Tucson and decided on the responsibilities for each of the major components in the warm part of the Band 6 cartridge. A block diagram that provides details is at

http://almaedm.tuc.nrao.edu/forums/alma/dispatch.cgi/iptfedocs/showFolder/100428/def/def/9049706

Continued updating wiring diagrams for the cartridge test system's temporary mixer-preamp bias supply. Tod Boyd and Ron Harris are completing the wiring harness from the pods to the cartridge for this project. Alex Grichener now has LabVIEW controlling this bias supply using code written by the Tucson group.

Gene Lauria and I wrote a short memo describing the mixer-preamp stability measurements taken in June. The memo is at

http://almaedm.tuc.nrao.edu/forums/alma/dispatch.cgi/iptfedocs/docProfile/100433/d20030822184212/No/t100433.htm

Ralph Groves completed measurements of another 2SB mixer-preamp.

Name: Wes Grammer
IPT: Front End

OMT development:

a. George Reiland has taken change of this task - this is my last report.
b. Fabrication of the production Band 6 OMT is underway at J&E.
c. Design of flange adapters for testing the production Band 6 OMT with electroformed transitions and adapters fabricated for 1mm Test OMT is completed will go out for fab soon.

Front End work:

a. Finished revising Band 6 cartridge-to-bias module internal ICD.
b. Reviewed and commented on several other FE ICDs.
c. Worked on design and component selection of analog data acquisition portion of Cartridge Bias Module.
d. Attended several meetings and telecons regarding Front End issues.

Name: Gene Lauria
IPT: Front End

4-12 GHz amplifiers: Mike Lambeth has finished the construction of 4 amplifiers, and they will be ready for testing by the end of Friday (8-22). The kits for the 3 amplifiers to be built at ACC will be sent out early next week.

Mixer/preamp Test Dewar: The Dewar now has power, all the necessary feedthroughs for bias & power, and heaters. Kirk Crady has made all almost all of the cables that go between the rack electronics and the Dewar, and will finish the remainder this week. The drawings for the brackets that will hold the feedhorn and mixer have been submitted to our machine shop, and Mark Wharam has started making them. A cooldown has been performed, and a minimum temperature of 3.5 K was achieved on the second stage in about 3.25 hrs. time. Full equilibrium was achieved in 4 hrs. time. Heat was applied to the 4 K plate until the temperature went to 4.2 K, and an excess of about 0.75 W was measured. It looks like there should be enough capacity to accommodate the rest of the components which would include the mixer/preamp (which will dissipate about 17 mW), and the LO waveguide. The heaters were tested, and the Dewar warms up to room temperature in 1.25 hrs.

Name: Kamaljeet Saini
IPT: *Front End*

(I.) ALMA Work Element Sheet WBS: 4.255.1800:

1) Completed the technical write-up, specifications, delivery schedule and sole source justification for a request for quote for the supply of cooled final stage LO frequency multipliers for Bands-6, 7 and 9 from Virginia Diodes Inc. (VDI)
To Do: Some "TBD" items are still awaiting final decision, pending some new amplifier tests, before it can be finalized by the business office and set out to the vendor.
2) In the meanwhile, VDI has provided a quote based on discussions with them two weeks ago. The prices quoted are being evaluated.
3) Andrey Baryshev (SRON) completed evaluation of a band-9 quintupler (using the UVA Carlstrom Gunn-oscillator that was shipped out to him last week) with his Band-9 SIS receiver. His conclusion (with some caveats) was that with 30 mW input pump power to the quintupler, there appears to be enough power generated at the output of the quintupler to pump the SIS mixer sufficiently. Considering all the other losses between the LO driver amplifier output and the frequency quintupler input, it is almost certain that the new 30 mW output amplifiers will need to be power-combined for the frequency quintuplers to be viable.
4) Started work on putting together the new stand alone frequency multiplier cryogenic test station. All the hardware and software on order for this task was received earlier this week.

(II.) Other/Miscellaneous Tasks:

1) John Webber called a meeting to solicit suggestions for the proposed Observatory wide workshops/conferences. Emailed suggestions/opinions in that regard.
2) LO group meeting on Thursday to discuss the new VDI quote and finalize the specifications for a formal "RFQ".

Name: Chris Langley
IPT: Back End Data Transmission System

1. DTX Builds

Mario Torres and Greg Chavez have agreed to populate 5 digital transmitter cards for bench development and system integration. They will accomplish this mostly after hours. I had originally planned to out source this work, but after considering the cost of this plus the fact that these two are very experienced with the techniques necessary to successfully produce a working card, the decision to have these cards populated in house was the logical one.

Firmware work is still required to complete the digital transmitter. Code for monitor and control points still need to be developed.

2. PS/MC card builds

Aubrey Erickson (student hire) has been given the task of populating five power supply / monitor control boards for the transmitter modules and bench top tests. He will work on this job as his time allows.

3. DTR builds

Selina Sutton is spearheading the effort to populate the digital receivers necessary for bench testing and system integration. One card was successfully assembled and sent to JBO. Unfortunately, the second card built up has not met the same success. Three days of troubleshooting on my part has not yet produced a working receiver.

The problems with this card seem two-fold. First, we tried to incorporate some time saving measures. Instead of using the paste dispenser to individually apply paste to each demultiplexer pad (ceramic BGA), we attempted to use the board stencil and re-flow oven to install these parts. We have met with limited success using this method in the past, and it was hoped that we could successfully use this technique at this time. Unfortunately, two of our demultiplexers appear to be in need of re-installation.

Also, a very interesting problem with one data channel is present on this card. Inside that channel's FPGA, the system clock is being shut down at every one 100,000th of its period. We tried the card with system clocks of 125 MHz and 128 MHz with the same results. At this time it does not appear the FPGA code is producing this anomaly. Another receiver card is being populated at present, and it should be ready to test next week. Needless to say, I am somewhat relieved that we had already produced one fully functional digital receiver.

Monitor and control code still needs to be implemented in the receiver FPGAs.

4. Modules

I have ordered several aluminum cover plates for the receiver assembly. These will hold the Diamond E2000 back plane connector blocks and excess fiber spool. I expect delivery by the middle of September.

The front plate for the transmitter module has been redesigned to suit ALMA's requirements (as opposed to EVLA's). Module hardware for system integration still needs to be ordered.

I have been in contact with Guy Montignac (Bordeaux) concerning the mounting of their sampler/digitizer assembly in the transmitter module. I have sent him a drawing of the module's center plate with mounting hole locations and he has responded with a drawing of his own (iterative process). I have not had a chance to go over his design, as yet.

5. Transmitter Transponder Design

Kerry Shores has begun routing the card. I have provided him with several schematic changes in the past week, and I'm sure I'll be giving him more changes before requesting a review of this design.

6. DTS Test Set

Work continues slowly on this project. Nico Marrero continues to build the schematic as I feed him system requirements.

Name: Chip Scott
IPT: Back End

Monitor and Control:

The Herotek DZR185AA detectors arrived this week. These detectors are to be used to monitor the output power of the DYTO and power amplifier output. Actually, it is monitoring the phase lock loop power level since it is on the other output of the power splitter on the coupled port of the coupled power dividers (CPD).

Originally, I had two reasons for wanting to monitor the power levels here. First, I assumed that the phase lock loop would be sensitive to the power level of the loop signal which drives the LO port of the mixer (the RF port is driven by the reference comb lines). If the LO power drops too low, then the loop should drop out of lock. Secondly, if the DYTO or power amplifier is beginning to fail, then the power level would drop and so this monitor would function as a component failure alarm (when the detected voltage was routed to an M&C window detector).

To test the detectors, I installed one as described above. I added a step attenuator between the output of the lowpass filter (after the power amp) and the input of the CPD. For normal operation, I expect the power level in the loop to be 7 ± 3 dBm (or 4 to 10 dBm). For these power levels, the detector voltage is between about –0.5 and –1.1 volts.
I repeated the test for a second randomly selected detector and got the same readings within a few milli-volts.

The surprising part of this test was when I tried to find the power level when the PLL would stop locking. The loop power is nominally 7 dBm. The loop power is used as the LO power for a mixer which requires 7 dBm drive power. But, when I drop the power (using the step attenuator) the loop lock detector showed lock and the spectrum analyzer signal showed a signal that appears to be locked when the step attenuator was set as low as –35 dB. This means the PLL stays locked when the LO power level drops as low as –28 dBm!

I am not quite sure how this is possible but the test results were clear. Apparently, there is no chance the PLL will go out of lock due to low LO power levels unless there is a

catastrophic failure of the DYTO or power amplifier. There is a possibility of a greater propensity for false locking but this has not been verified (nor do I see a need to verify it).

LO and Timing:

I have pounded out my first draft of the LO and Timing Design Specifications and Requirements documentation (BEND-50.03.00.00-001-A-SPE). I will forward to Bill Shillue and Rob Long for comments and inputs.

Name: Scott Rankin

IPT: Computing

Progress

* Assisted Control subsystem with integration issues.
* Assisted Control subsystem with CVS issues.
* Collected information on I&T tools and processes.
* Reviewed ALMA Software Integration, Test and Support Plan
* Reviewed ALMA Science Requirements and Use Cases.
* Asked HR to re advertise vacant SE position Software Engineer (SO2470).
* Started filtering resumes for vacant Software Engineer (SO2470) position.
* Started trying to duplicate I&T's monthly integration process.
* Started collecting requirements for I&T portion of ALMA Software Test Plan.
* Picked up new assignments from Correlator subsystem.

Issues

* None

Activities

* Complete filtering resumes for vacant Software Engineer (SO2470) position.
* Complete I&T portion of ALMA Software Test Plan for R1.0.
* Complete Correlator subsystem development work for R1.0.
* Publish ALMA GUI Style Guidelines for review.
* Plan October trip to Garching to support R1.0 integration.
* Develop supporting software for ALMA GUI Style Guidelines.
* Develop ALMA 3rd Party Library Collection.
* Document Linux Dynamic linking mechanism.