ALMA Weekly Progress Report
15th August 2003

Name: Jeff Mangum
Group: AEG

ATF:

1. Continued characterization of VertexRSI antenna positioning system.
2. Received some diagnosis instruction from VertexRSI regarding disfunctionality of tiltmeter system. Will look into this next week.
3. Re-analyzed VertexRSI radiometer system installation date with Pokorny, Marson, and Perfetto. The new start date for installation is 2003/09/15.

ALMA:

1. Submitted several ALMA Design Reference Science Plan projects to Al Wootten for inclusion in the general plan.
2. Reviewed a nice document by Richard Hills which describes some very useful OTF scanning modes.
3. Reviewed an update to ICD 11 (Antenna Coordinate Systems) by Eric Pangole.
4. Reviewed ALMA Memo 461, "The Calibration System Revisited", by Guilloteau and Bacmann.

Other:

1. Updated Tucson REU page (http://www.tuc.nrao.edu/education/students/NRAOstudents_tuc.shtml).
2. Wrote the Tucson REU program summary for John Hibbard's NSF report.

Name: John Effland
IPT: Front End

1. Obtained some data from another round of saturation measurements until the JT-2 Dewar froze out. Results were documented in a memo.
2. Analyzed gain slope and wrote memo summarizing the reasons why the Band 6 group feels the real parameter of interest is the spectral density within any 2-GHz band. The memo shows that this parameter is +/- 4.5 dB for Band 6.
3. Generated and distributed a drawing that defines responsibilities for components installed on warm side of Band 6 cartridge.
4. Updated and returned the "Band 6 Cartridge to IF Switch" ICD to Hans Rudolf.
5. Generated harness wiring diagram to connect Tucson's temporary bias electronics to the Band 6 cartridge.
6. Revised and returned to Wes Grammer the latest version of the Band 6 Cartridge to Bias Electronics ICD.

Name: Gene Lauria
IPT: Front End

4-12 GHz IF Amplifiers: Met with Charles Brand who is the CEO of Advanced Control Components, and gave him our documentation on the construction of the IF amplifiers. We went over some details while he was here, and he is going to review them and report back to me if there are any further questions. He has confirmed his quote first given in February for the price of the construction. Mike Lambeth is putting together a few more pieces for the parts kit that will be sent to ACC for the first 6 amplifiers. The kits should go out by the end of the week. Also, Mike is building up 4 more amplifiers for further mixer evaluation.

Mixer/Preamp Test Dewar: Sumitomo forgot to send us the power cable which connects the main 3-phase power to the compressor. They sent it last week, and it should be here by Monday or Tuesday the latest. They have also sent the spare cold head which wasn't expected to be delivered until October, so they are far ahead of schedule for the delivery of the cold head. The power and helium lines have been run to the test Dewar, and it is ready for a cooldown. However, an additional 3-phase service had to be installed to run the compressor. The electrician has been in the lab installing the service, but they haven't finished yet. They should be finished early this week. The Dewar was pumped down last Friday to check for leaks, and only a few minor ones were found and repaired. The hermetic connectors for the wiring for the Dewar are mostly finished. There will not be any electronics inside the Dewar for this cooldown. It is just a test to see how the refrigerator performs with the new mixer and the head load of the wiring. All of the optics have been installed and aligned with a laser. The bracketry to hold the mixer/preamp assembly is being drawn up and should be submitted into the shop this week. Unfortunately though, the cables that go between the rack electronics and the Dewar will have to be made over because the cables are too short with the new layout of the Dewar. Kirk Crady is going to make the new cables, and they should be done in two-week's time. These cables are not on a critical path, so it shouldn't impede progress. If the power is available and the cable delivered early this week, a cooldown should be started by mid-week.

Name: Kamaljeet Saini
IPT: *Front End*

(I) ALMA Work Element Sheet WBS: 4.255.1800

1) Writing specifications for developing a request for quote from Virginia Diodes Inc., for the cold first LO frequency multipliers for Bands-6, 7 and 9. Spent time on soliciting input from representatives of the various bands on the current specifications, and if those are acceptable for future.

To Do: Once the information gathering phase is over, need to write down all the specifications in some detail for the RFQ.

2) VDI inquired about the payment for the prototype frequency multiplier order. Payment has been released for the triplers supplied for bands-6 and 7, but held up for the five band-9 quintuplers. Charles and Andrey are working on getting the band-9 mixer test results as soon as possible, which will allow for a decision to be made.

3) Released the following mechanical drawings as ALMA EDM documents:

FEND-40.10.00.00-010-A-DWG: Band-6 Cold Frequency Tripler (Prototype) - Outside Mechanical Details

FEND-40.10.00.00-007-A-DWG: Band-7 Cold Frequency Tripler (Prototype) - Outside Mechanical Details

FEND-40.10.00.00-008-A-DWG: Band-9 Cold Frequency Quintupler (Prototype) - Outside Mechanical Details

4) **To Do:** Waiting for the delivery of LabVIEW software to begin configuring the new setup. Order was sent out to the software vendor two weeks' ago.

(II) Other/Miscellaneous Tasks:

1) Group meeting on Monday afternoon to discuss the viability of upcoming milestones. Presented a brief summary of the meeting with VDI on Thursday last week.

2) Completed testing the modified band-pass filters for first LO driver chains. There was a marked improvement in performance noticed as a result of modifying the metal-housing covers. Consolidated all of the band-pass filter measurements (all four bands plus a band-6 test set design variation) into a test report for easy future reference. Available as ALMA EDM document number FEND-40.10.00.00-009-A-REP.

To Do: Though usable as of now, the filters could be improved by modifying the mask at a future date to take into account the effects of over-etching of the photo-lithographic pattern. The over-etching was close to manufacturer specified tolerance but was still significant enough to result in some change in pass-band frequencies. See test-report for further details.

3) Meeting with Porter Thompson (Skip Thacker's summer student) on Friday to review the operational details of his stand-alone LO control module.

Name: Eric Bryerton
IPT: Front End / Local Oscillator

Band 7 Lab Prototype LO will be shipped to IRAM Monday. Problem with bias cards resetting has been solved.

InP power amplifier MMIC wafer run is complete. Initial PCM tests look very good. Wafer is diced and being sent to JPL for probe testing. At the same time, chips are being sent here to be packaged and tested.

Name: Bill Shillue
IPT: Back End / Local Oscillator

Christophe Jacques joined the LO photonic group as an engineer specialist in photonics. Week of Aug 4-8: Conducted tests of the line length correction system on the ATF Vertex antenna. The system was able to track the fastest changes in fiber phase due to antenna motion and vibration. However the measured microwave phase was not zeroed, and displayed a dependence on the antenna AZ-EL position. The reason for this is not understood.
Next week we will dig into the data and try to figure it out. Week of Aug 11-15: Laser Synthesizer Test using a stabilized master laser and a tunable DFB fiber laser locked via an external fiber frequency shifter. This test is ongoing through Aug 27th. The main goal of demonstrating low phase noise has already been met albeit at low (450 MHz) frequency. Next we will demonstrate that this is extendable to 142 GHz and meeting ALMA phase noise spec.

Name: Chip Scott
IPT: Back End

2nd LO Synthesizer Bench Test Plan:
The Hameg Quad power supply was delivered this week. This power supply was used to replace the various bench power supplies. The power supply was used to supply ±16.5V and ±6.5V to the 2nd LO Synthesizer regulator board. The complete circuit included the Herotek comb generator module and crystal oscillator used in the test but actually provided by the LORR. The circuit was missing the AMBSI2 board on the FTS and the Monitor and Control board does not exist, yet. The 2nd LO Synthesizer was tuned to the highest frequency, since the DYTO draws the most current at this frequency. The current draw of the circuit is compared to the previous estimate of current draw in the table below.

Voltage/Current	+16.5V	-16.5V	+6.5V	-6.5V
Actual	1.822 A	0.178 A	0.351 A	0.008 A
Estimated	2.579 A	0.804 A	0.726 A	N/A

The current draw estimate for the ±16.5V supply includes about 300 mA for the YIG heater, which is on only for about the first 30 seconds of operation. No change in the spurious levels of the synthesizer were seen and remained less than –70 dBc.

Monitor and Control:

The monitor portion of the monitor and control board design is very solid in my mind. I currently plan to monitor the regulated voltages ±15V and ±5V with On Semiconductor MC33161 Universal Voltage Monitors configured as window detectors with a logical True output if the voltages fall within the window. The output power of the DYTO is detected at one of the power divider ports on the coupled port of the Coupled Power Dividers using a Herotek DZR185AA detector. The (negative) detected voltage is routed to the M&C board. An MC33161 Universal Voltage Monitor configured as a window detector has a logical True output when the sampled power is within a +7 ± 3 dBm power window. The IF and FTS power are monitored using couplers on the PLL PCB. The IF and FTS samples are routed to the M&C board. Cougar DTS4001 threshold detectors are set to a threshold of –30 dBm and will have a logical true if the power is above the threshold. The lock detector of the PLL PCB has logic for three mutually exclusive states: above lock range, below lock range, or locked. These logic signals are also routed to the M&C PCB.

The control aspect is a little less clear. I am torn between total computer control and some low level of 2nd LO autonomy. According to Ralph Marson, I cannot expect the computer to provide too much control since the control is not real time nor even that fast. I am seriously thinking about the 2nd LO handling the task of switching the Tune/Lock switch of the synthesizer based upon some sort of counter/delay in the FPGA instead of computer controlling this switch. At the same time, I might want to include a diagnostic flag where the computer could control the switch if it was in this diagnostic mode. The design of the control aspect continues.

LO and Timing:

I have started looking at the LO and Timing Design Specifications and Requirements documentation (BEND-50.03.00.00-001-A-SPE).

Name: Jim Pisano
IPT: Computing

Completed a preliminary test which extracts raw lags from the correlator and coverts them to spectra. The spectral results agree with tests made by the hardware engineers. This test validates the basic functionality of the CDP, namely the data flow through the CDP software from the hardware interface port to spectral data.